ELECTRONIC DEVICES & CIRCUITS
Module 5

OP-AMP- 1

S3 CSE KTU

prepared by

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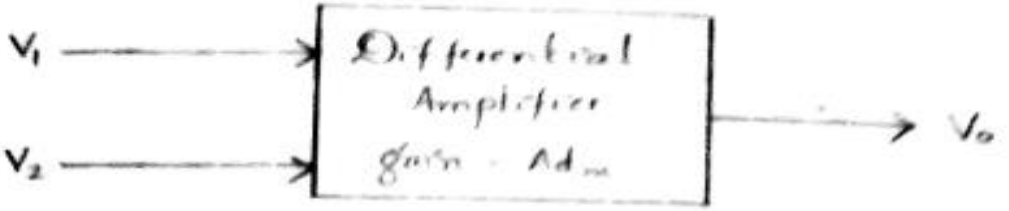
DIFFERENTIAL AMPLIFIER

INTRODUCTION

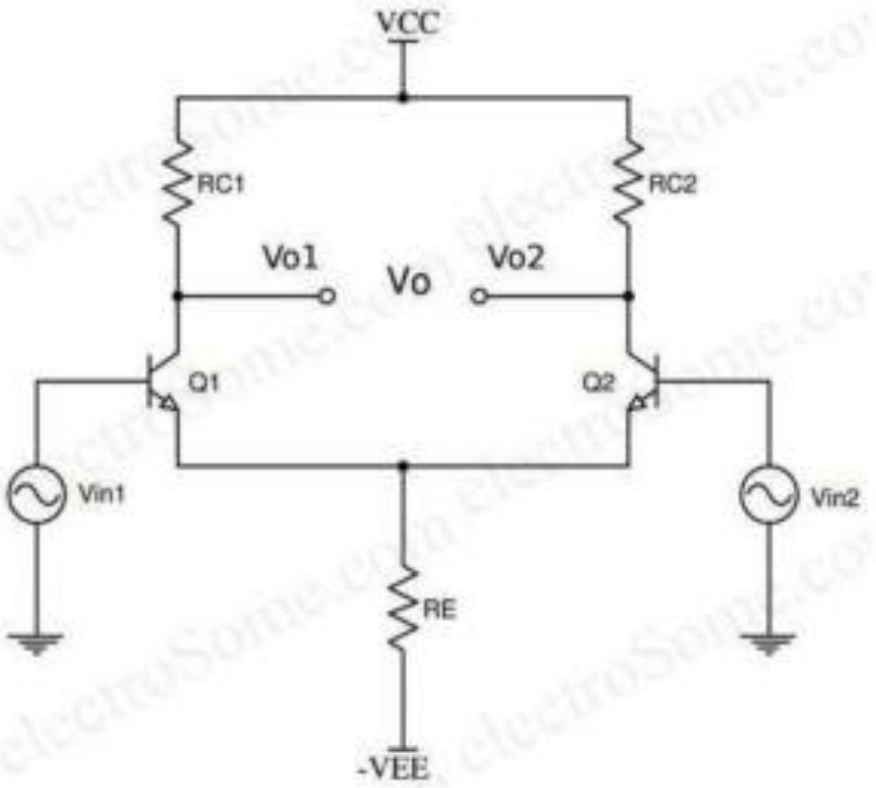
- As the name indicates Differential Amplifier is a dc-coupled amplifier that amplifies the difference between two input signals.
- It is the building block of analog integrated circuits and operational amplifiers (op-amp).
- One of the important feature of differential amplifier is that it tends to reject or nullify the part of input signals which is common to both inputs.
- This provides very good noise immunity in a lot of applications.



$$V_o = A_{dm}(V_1 - V_2)$$

DIFFERENTIAL AMPLIFIER USING BJT

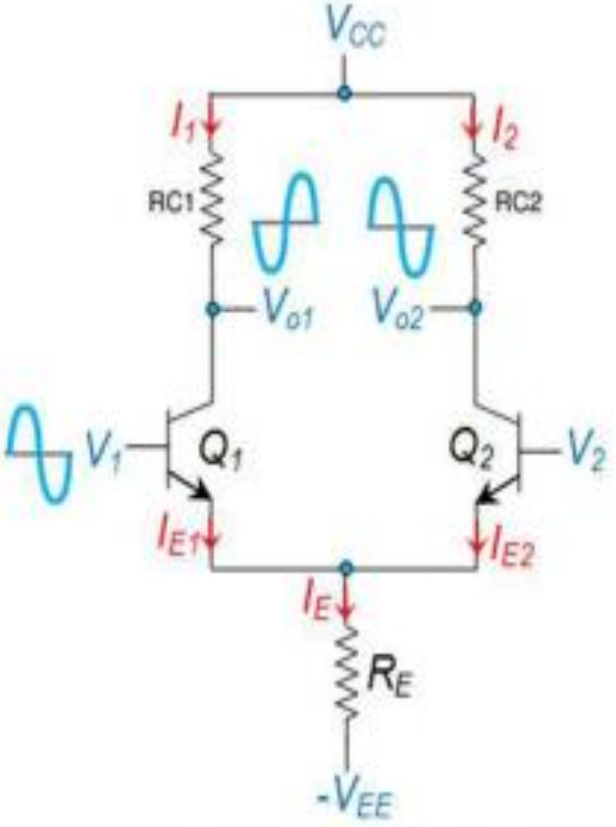
- The simplest form of differential amplifier can be constructed using Bipolar Junction Transistors as shown in the below circuit diagram.
- It is constructed using two matching transistors in common emitter configuration whose emitters are tied together.
- V_{i1} and V_{i2} are input terminals and V_{o1} and V_{o2} are output terminals with respect to ground.



The two transistors Q_1 and Q_2 have identical characteristics. The collector & emitter resistances of the circuit are equal, i.e. $R_{E1} = R_{E2} = R_E$, $R_{C1} = R_{C2}$ and the magnitude of $+V_{CC}$ is equal to the magnitude of $–V_{EE}$. These voltages are measured with respect to ground.

WORKING

- Figure shows a circuit made of two BJTs (Q_1 and Q_2) and two power supplies of opposite polarity viz., V_{CC} and $-V_{EE}$ which uses three resistors among which two are the collector resistors, R_{C1} and R_{C2} (one for each transistor) while one is the emitter resistor R_E common to both transistors.
- Here the input signals (V_1 and V_2) are applied to the base of the transistors while the output is collected across their collector terminals (V_{o1} and V_{o2}).



A BJT Differential Amplifier

When a differential amplifier is driven at one of the inputs, the output appears at both the collector outputs

- **In this case, if the V_1 at Q_1 is sinusoidal, then as V_1 goes on increasing, the transistor starts to conduct and this results in a heavy collector current I_{C1} increasing the voltage drop across R_{C1}, causing a decrease in V_{o1}.**
- **Due to the same effect, even I_{E1} increases which increases the common emitter current, I_E resulting in an increase of voltage drop across R_E.**
- **This means that the emitters of both transistors are driven towards positive which inturn implies that the base of Q_2 would start to become more and more negative.**
- **This results in a decrease of collector current, I_{C2} which inturn decreases the voltage drop across the collector resistor R_{C2}, resulting in an increase in the output voltage V_{o2}.**

- **This indicates that the changes in the sinusoidal signal observed at the input of transistor Q_1 is reflected as such across the collector terminal of Q_2 and appear with a phase difference of 180° across the collector terminal of Q_1.**

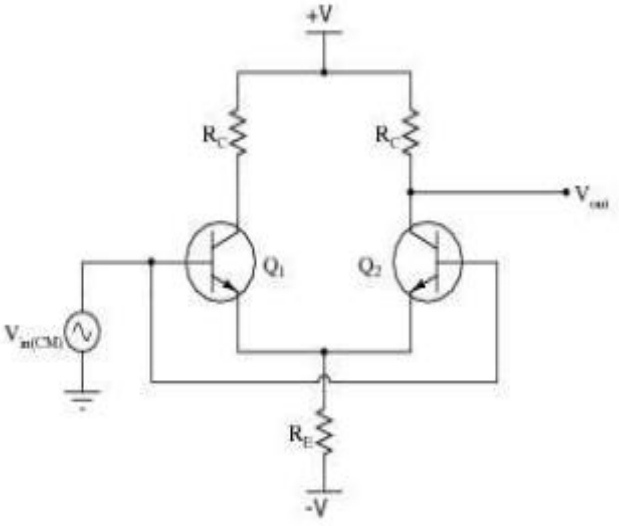
The amplification can be driven differentially by taking output between the collector of Q1 and Q2.
When two voltage sources V_1 & V_2 are connected to the base of both transistors, the difference between the two voltages is amplified.

O/P voltage is given by $V_0 = A_d(V_1 - V_2)$

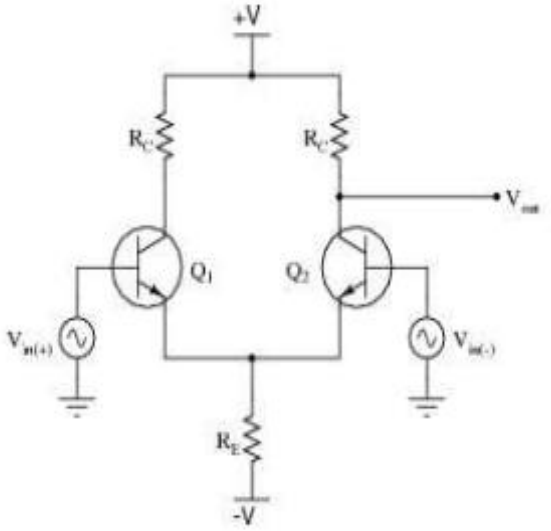
A_d refers to its differential gain.

COMMON MODE Vs DIFFERENTIAL MODE

- **COMMON MODE**



- **DIFFERENTIAL MODE**



Common mode connection
Ideal case: o/p should be = 0 since $(V_1-V_2) = 0$

But this does not happen. There is an o/p voltage which corresponds to the common mode component.

Common mode component :
$V_{cm} = (V_1+V_2)/2$

Differential mode component :
$V_d = (V_1-V_2)$

The common mode amplification output voltage given by

$$V_0 = A_C\left(\frac{V_1 + V_2}{2}\right)$$

A_C is called the common mode gain of the amplifier.

the mathematical expression for the output of the differential amplifier can be given as

$$V_0 = A_d(V_1 - V_2) + A_C\left(\frac{V_1 + V_2}{2}\right)$$

Thus, functionally-good difference amplifiers are expected to exhibit a high common mode rejection ratio (CMRR) and high impedance.

CONFIGURATIONS

- **We can feed two input signals at the same time or one at a time.**
- **In the former case it is called dual input, otherwise it is single input.**
- **Similarly there are two ways to take output also.**
- **If the output is taken from one terminal with respect to ground, it is unbalanced output or if the output is taken between two output terminals, it is balanced output.**
- **Based on the methods of providing input and taking output, differential amplifiers can have four different configurations as below.**

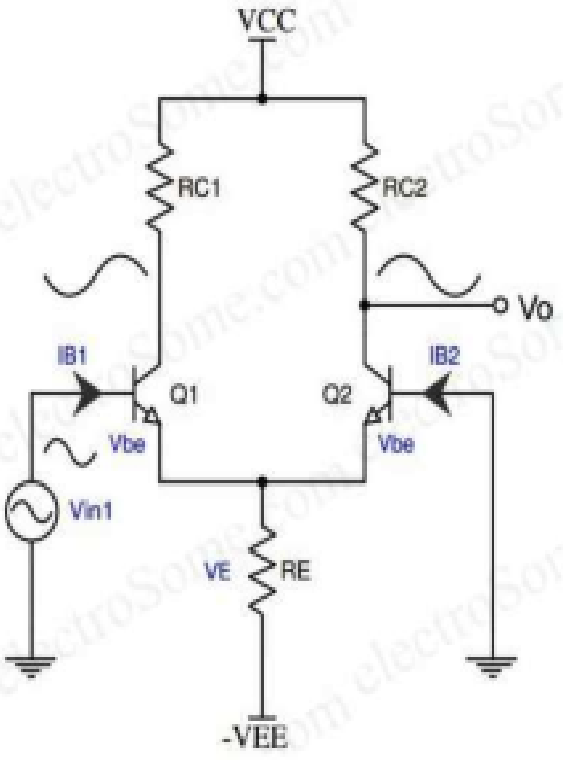
1. **Single Input Unbalanced Output**
2. **Single Input Balanced Output**
3. **Dual Input Unbalanced Output**
4. **Dual Input Balanced Output**

If the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground.

If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output.

SINGLE INPUT UNBALANCED OUTPUT

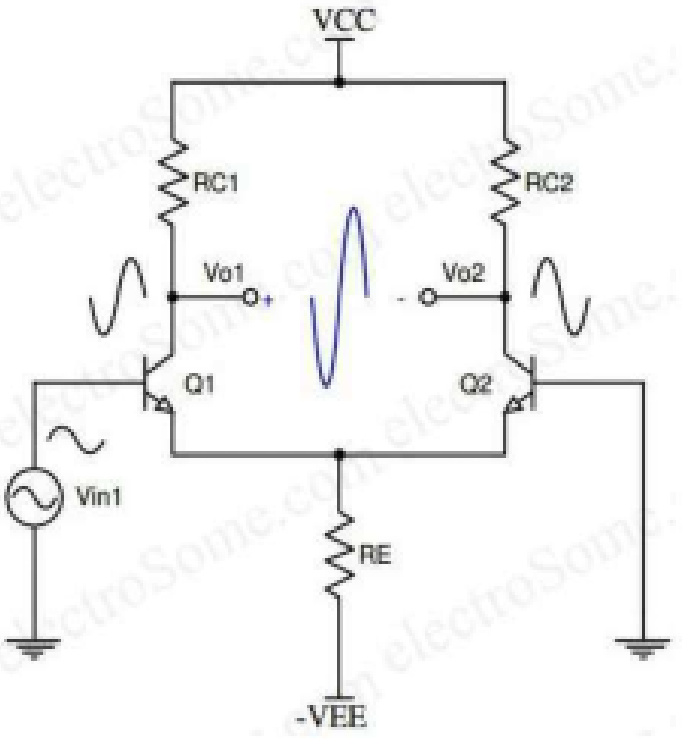
- In this case, only one input signal is given and the output is taken from only one of the two collectors with respect to ground as shown below.
- When input signal V_{in1} is applied to the transistor Q1, it's amplified and inverted voltage gets generated at the collector of the transistor Q1.
- At the same time it's amplified and non-inverted voltage gets generated at the collector of the transistor Q2 as shown in the above diagram.
- Unbalanced output will contain unnecessary dc content as it is a dc coupled amplifier therefore this configuration should be followed by a level translator circuit.
- The effect of input voltage V_{in1} is coupled to the transistor Q2 via the common emitter resistor R_E.



Differential Amplifier using Transistor – Single Input Unbalanced Output

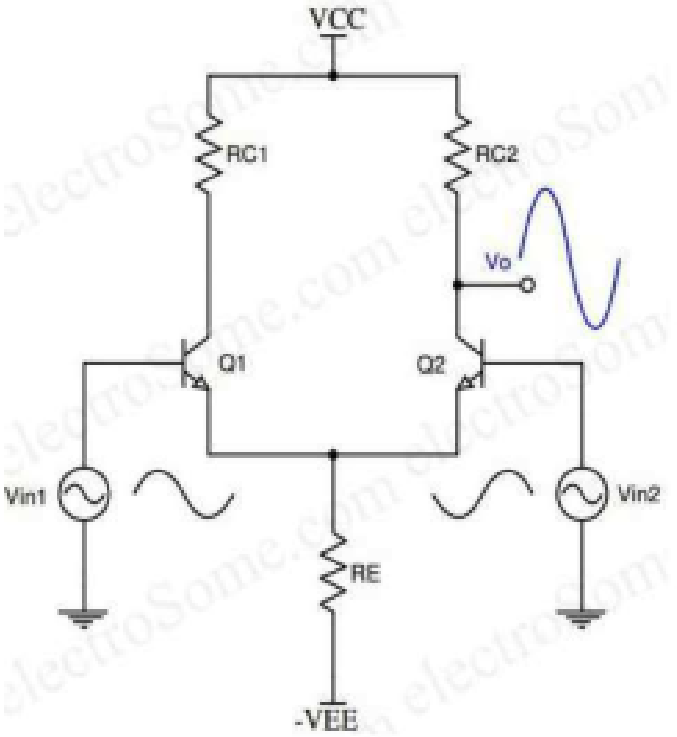
SINGLE INPUT BALANCED OUTPUT

- **As in single input unbalanced output, only one input signal is given even though the output is taken from both collectors.**
- **This will give us more amplified version of output as it is combining the effect of both transistors.**
- **There won't be any unnecessary dc content in balanced output as the dc contents in both outputs gets canceled each other.**
  - ***Vo = Vo1 – Vo2***



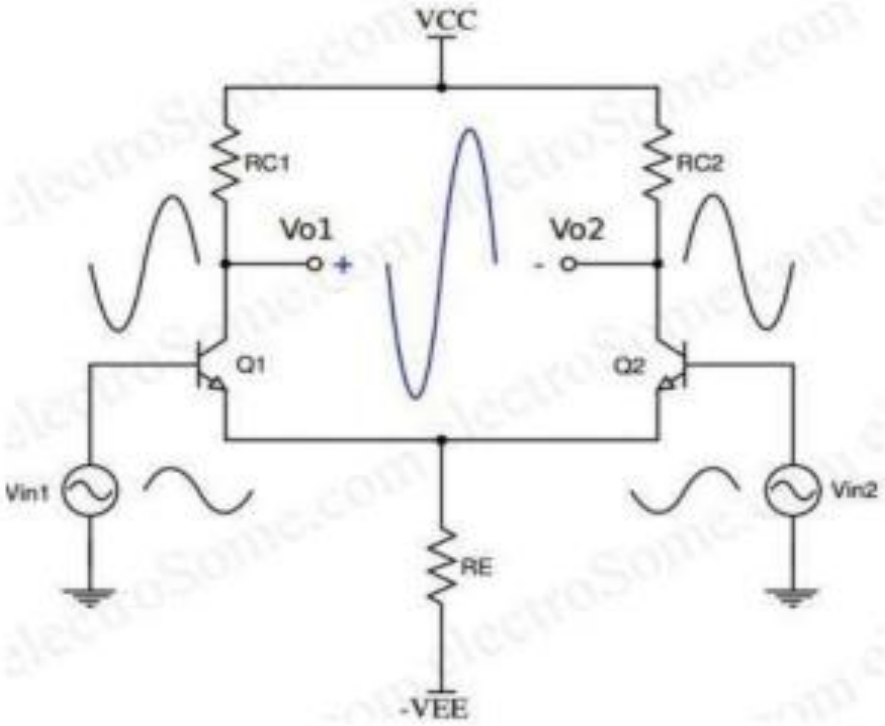
DUAL INPUT UNBALANCED OUTPUT

- **Both inputs are given in this case ie, differential input but the output is taken from only one of the two collectors with respect to ground as shown below.**
- **Amplified version of difference in both signals will be available at the output.**
- **The voltage gain is half the gain of the dual input, balanced output differential amplifier.**
- **Unbalanced output will contain unnecessary dc content as it is a dc coupled amplifier therefore this configuration should be followed by a level translator circuit.**



DUAL INPUT BALANCED OUTPUT

- Circuit consists of two identical transistors Q_1 and Q_2 with its emitters coupled together.
- Collectors are connected to main supply V_{CC} through collector resistor Rc.
- Magnitude of power supplies V_{CC} and $-V_{EE}$ will be same.
  - $Vo = A_d(Vin1 - Vin2)$
- Where Ad = differential gain
- Vin1, Vin2 = input voltages



COMMON MODE REJECTION RATIO (CMRR)

- **Dual input balanced output differential amplifier should suppress the common signals present at its inputs.**
- **A differential amplifier is said to be in common mode when same signal is applied to both inputs and the expected output will be zero.**
- **Effectiveness of rejection depends on the matching of two common – emitter stages used.**
- **The ability of a differential amplifier to reject common mode signal is called Common Mode Rejection Ratio (CMRR).**
- **Ideally output will be zero in common mode which implies infinite CMRR.**

The CMRR is defined as the ratio of the differential gain to the common-mode gain

$$\mathbf{CMRR = |Ad/Ac|}$$

CMRR is expressed in dB in data sheets

$$\mathbf{CMRR = 20log|Ad/Ac|\ dB}$$

FEATURES OF DIFFERENTIAL AMPLIFIER:

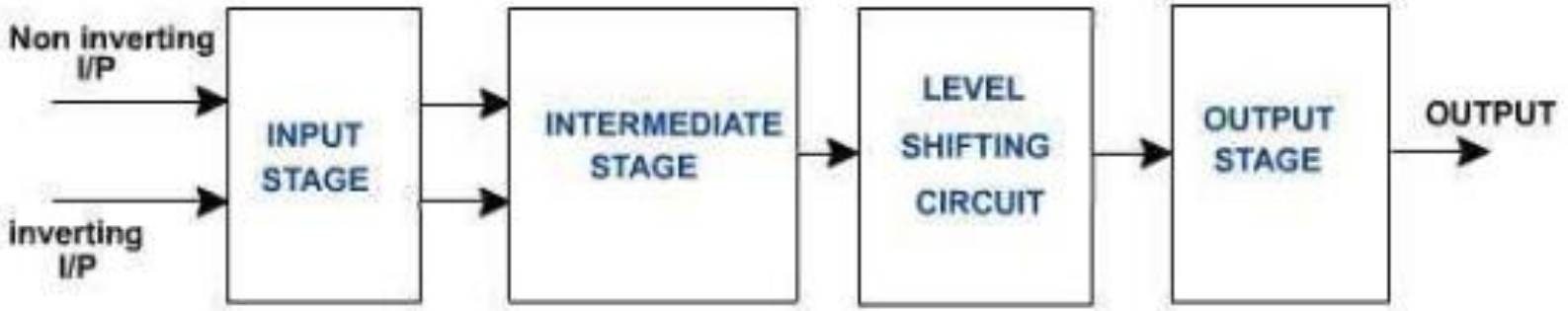
- **Differential voltage gain is high**
- **Common mode gain is low**
- **CMRR (common mode rejection ratio) is high**
- **Input impedance is high**
- **Wide bandwidth**
- **Low offset voltages and currents**
- **Output impedance is low**

OPAMP

INTRODUCTION

- It is a very high gain, high input impedance, direct coupled, negative feedback amplifier which can amplify signals having frequency ranging from 0Hz to 1MHz.
- An OPAMP is so called because they were originally designed to perform mathematical operations like
- summation,
- subtraction,
- multiplication,
- differentiation,
- integration etc.

OPAMP BLOCK DIAGRAM



- The input stage is a dual input balanced output differential amplifier.
- This stage provides most of the voltage gain of the amplifier and also establishes the input resistance of the OPAMP.

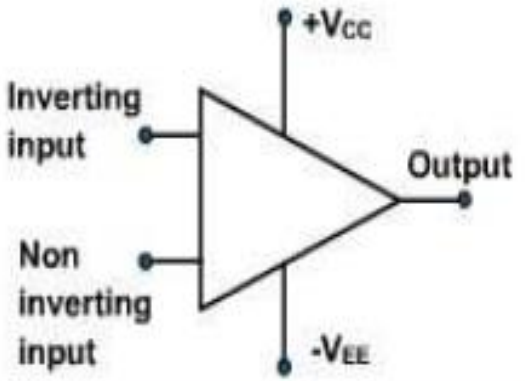
- The intermediate stage of OPAMP is another differential amplifier which is driven by the output of the first stage.
- This is usually dual input unbalanced output.
- Because direct coupling is used, the dc voltage level at the output of intermediate stage is well above ground potential.
- Therefore level shifting circuit is used to shift the dc level at the output downward to zero with respect to ground.
- An emitter follower with voltage divider is the simplest form of level translator.
- The output stage is generally a push pull complementary amplifier.
- The output stage increases the output voltage swing and raises the current supplying capability of the OPAMP.
- It also provides low output resistance.

IDEAL OPAMP CHARACTERISTICS

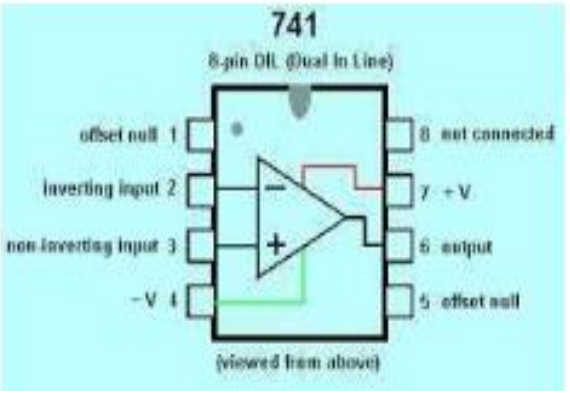
- An ideal OPAMP would exhibit the following electrical characteristic.
- Infinite voltage gain A_d
- Infinite input resistance R_i, so that almost any signal source can drive it and there is no loading of the input source.
- Zero output resistance R_O, so that output can drive an infinite number of other devices.
- Zero output voltage when input voltage is zero.
- Infinite bandwidth so that any frequency signal from 0 to infinite Hz can be amplified without attenuation.
- Infinite common mode rejection ratio so that the output common mode noise voltage is zero.
- Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

PRACTICAL OPAMP

- The symbolic diagram of an OPAMP is shown in figure below.



- 741c is most commonly used OPAMP available in IC package.
- It is an 8-pin DIP chip.

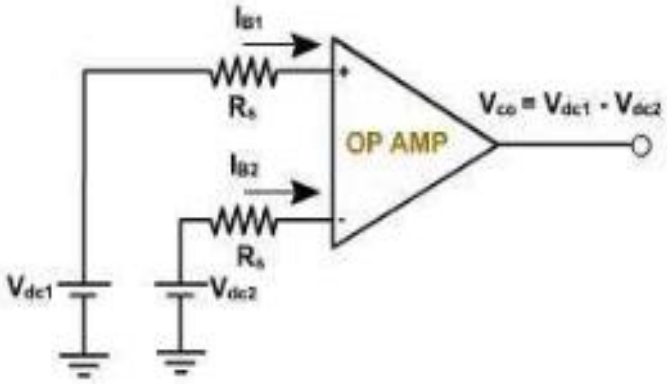


PARAMETERS OF OPAMP

1. Input Offset Voltage
2. Input offset Current
3. Input Bias Current
4. Differential Input Resistance(R_i)
5. Voltage Gain
6. Common Mode Rejection Ratio (CMRR)
7. Supply voltage Rejection Ratio (SVRR)
8. Output Resistance(R_O)
9. Bandwidth
10. Slew Rate

INPUT OFFSET VOLTAGE (V_{io})

- Input offset voltage is defined as the voltage that must be applied between the two input terminals of an OPAMP to null or zero the output
- V_{dc1} and V_{dc2} are dc voltages and R_S represents the source resistance.
- V_{io} is the difference of V_{dc1} and V_{dc2}.
- For a 741C OPAMP the maximum value of V_{io} is 6mV.



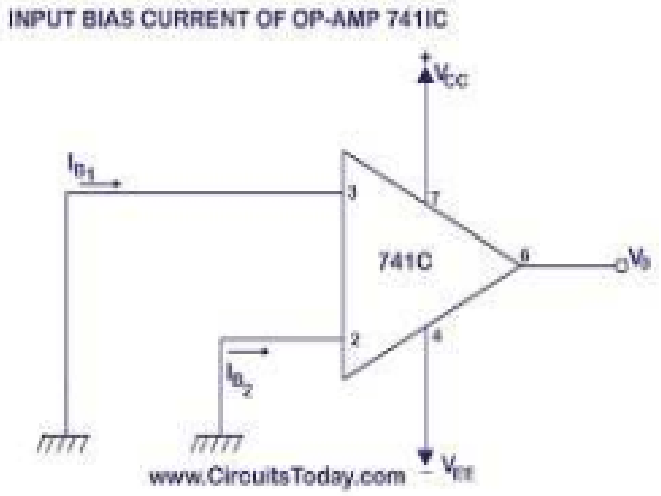
- The smaller the input offset voltage the better the differential amplifier, because its transistors are more closely matched.

INPUT OFFSET CURRENT(I_{io})

- Ideally, no current flows into the input terminals of an op amp.
- In practice, there are always two input bias currents, I_{B1} and I_{B2}
- The input offset current I_{io} is the difference between the currents into inverting and non-inverting terminals of a balanced amplifier.

$$I_{io} = |\ I_{B1} - I_{B2}\ |$$

- The I_{io} for the 741C is 200nA maximum.
- As the matching between two input terminals is improved, the difference between IB1 and IB2 becomes smaller, i.e. the I_{io} value decreases further
- For a precision OPAMP 741C, I_{io} is 6 nA



INPUT BIAS CURRENT (I_B)

- The input bias current I_B is the average of the current entering the input terminals of a balanced amplifier i.e.

$$I_B = (I_{B1} + I_{B2}) / 2$$

- For 741C, $I_{B(max)} = 700$ nA
- For precision 741C, $I_B = \pm 7$ nA

VOLTAGE GAIN

- **Since the OPAMP amplifies difference voltage between two input terminals, the voltage gain of the amplifier is defined as**

$$\text{Voltage gain} = \frac{\text{Output voltage}}{\text{Differential input voltage}}$$

$$A = \frac{V_o}{V_{id}}$$

- **Because output signal amplitude is much large than the input signal the voltage gain is commonly called large signal voltage gain.**
- **For 741C, the voltage gain is 200,000 typically.**

COMMON MODE REJECTION RATIO (CMRR)

- CMRR is defined as the ratio of the differential voltage gain A_d to the common mode voltage gain A_{CM}

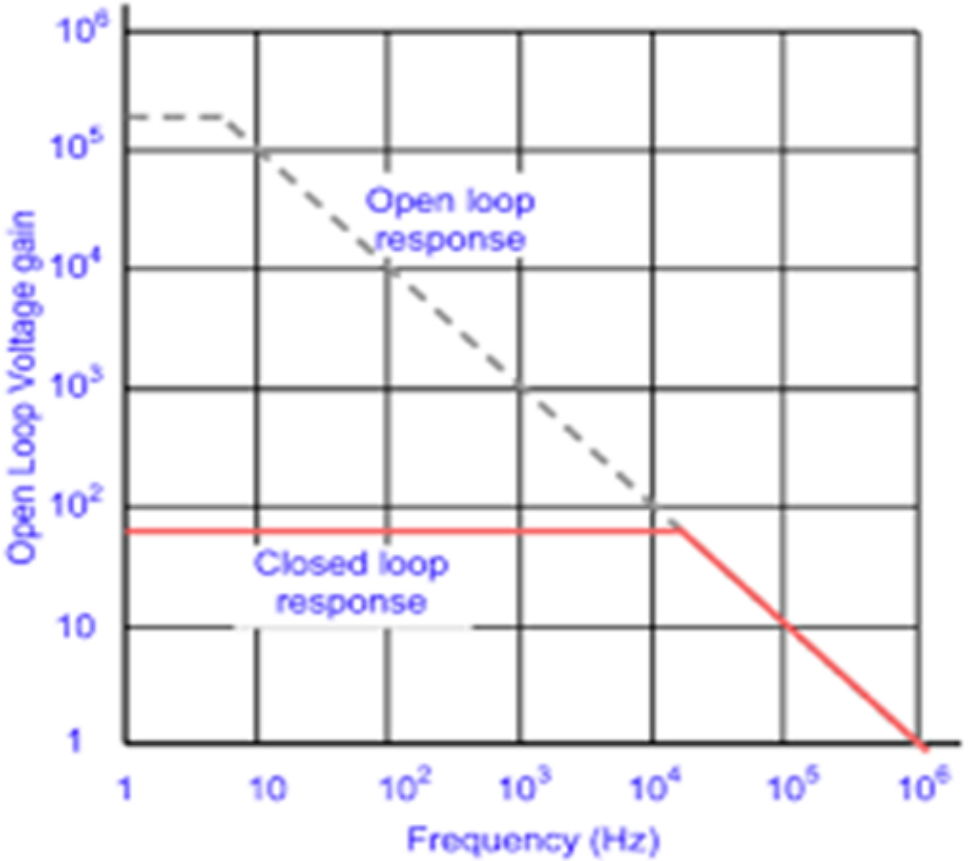
$$CMRR = A_d / A_{CM}$$

$$CMRR \text{ in dB} = 20 \log (A_d / A_{CM})$$

- For the 741C, CMRR is 90 dB typically.
- The higher the value of CMRR the better is the matching between two input terminals and the smaller is the output common mode voltage.

FREQUENCY RESPONSE

- The frequency response curve is shown in figure.
- The open loop gain is large at very low frequencies.
- From open loop gain vs frequency graph, it can be found that for the 741C OPAMP the gain reduces to 1 at a frequency of 1MHz (unity gain frequency, which is the maximum usable frequency) .
- Beyond 1MHz, the gain of the OPAMP is 1.
- [illegible]



Product of the gain against frequency is constant at any point along the roll off curve for open loop and closed loop
This constant is generally known as the **Gain Bandwidth Product** or **GBP**.

GBP = Gain x Bandwidth = Ad x f
f = cut off frequency (Hz)
Therefore decreasing the gain by a factor of ten will increase the bandwidth by the same factor.
Also that the unity gain (0dB) frequency also determines the gain of the amplifier at any point along the curve.

SLEW RATE(SR)

- **Slew rate is defined as the maximum rate of change of output voltage per unit of time under large signal conditions and is expressed in volts / m secs.** or V / μs and is caused by a step change on the i/p

$$SR = \left.\frac{dV_o}{dt}\right|_{max} \quad V/mS$$

For example 1V/μS **slew rate** means that the output rises or falls by 1V in one microseconds

- **It is a measure of fastness of op-amp.**
- **Slew rate indicates how rapidly the output of an OPAMP can change in response to changes in the input frequency with input amplitude constant.**
- **For the 741C the slew rate is low 0.5 V / m S which limits its use in higher frequency applications.**

One of the important frequency related parameter of an op-amp is the **slew rate**

IDEAL VOLTAGE TRANSFER CURVE:

- **The graphic representation of the output equation is shown in figure in which the output voltage v_O is plotted against differential input voltage v_d, keeping gain A_d constant.**