1. Describe the evolution of Microprocessors.

During the evolution microprocessors advanced in 3 attributes.

* No: of transistors :- when transistors increase more logic circuits for implementing instructions are possible.

* Data Width :- It is the amount of data transfered through the internal bus of the processor and processed by ALU. When no: of bits in Data width increases the speed of the processor increases.

* Clock speed :- It denotes the frequency of processing inside the processor.

The following table shows the Evolution of Intel μps.

NAME	YEAR	TRANSISTORS	DATA WIDTH	CLOCK SPEED
8080	1974	6,000	8 bits	2 MHz
8085	1976	6,500	8 bits	5 MHz
8086	1978	29,000	16 bits	5 MHz
8088	1979	29,000	8 bits	5 MHz
80286	1982	134,000	16 bits	6 MHz
80386	1985	275,000	32 bits	16 MHz
80486	1989	1,200,000	32 bits	25 MHz
PENTIUM	1993	3,100,000	32/64 bits	60 MHz
PENTIUM II	1997	7,500,000	64 bits	233 MHz
PENTIUM III	1999	9,500,000	64 bits	450 MHz
PENTIUM IV	2000	42,000,000	64 bits	1.5 GHz

2. What do you mean by clock speed of a processor. What is the clock speed of 80869

* Also known as clock rate.
* Each processor depends on an external clock which generates clock cycles (clock ticks)
* The rate of this clock ticks regulate and synchronizes processing.
* The faster the clock, faster the processor.
* It is expressed in MHz or GHz.
* Clock speed of 8086 is f = 5 MHz to 10MHz. That means the time period of a single clock cycle is $T = \frac{1}{10MHz} = 0.1\ \mu s$.

3 Describe the register organization of 8086?

* 8086 has two sets of Registers which are of 16 bits.
  - General Purpose registers
  - Special purpose registers.
* General purpose Registers.
  - They are 16 bit registers.
  - They are AX, BX, CX & DX.
  - They can also be used as 8 bit registers.

	16 bit	
AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL
	8 bit	8 bit

* These registers are used for all kind of arithmetic and logical operations.
* They have other special duties as follows.

Cx - default counter.
Bx - offset register.
Dx - Destination register.

* Special Purpose Registers.

They are.
- Segment Register.
- Pointer Registers
- Index Register.
- Flag Register.

* Segment Register - CS, DS, ES, SS

These are the 16 bit registers used to store the base address of each segment.

Base Address Register	Segment.
CS	Code Segment.
DS	Data Segment.
ES	Extra Segment.
SS	Stack Segment.

* Pointer Registers. - IP, BP & SP.
  * These registers act as pointers in particular segments.
  * These registers point to a location by storing its offset value.

* IP stores the offset value in code segment.
* BP & SP stores the offset value in Stack segment.

* Index Registers - DI, SI.
  - There 16 bit registers are also used to store offset value.
  - They are also used to store index values in indexed, based indexed and relative base indexed addressing modes.
  - DI is used to store the offset of destination of data and SI is used to store the offset of source of data.

* Flag Register
  - This is also a 16 bit register that contains flag bits that indicate results of computations in ALU.
  - Some bits are used to control cpu operations.

[Draw the flag Register and note down the bits.]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	O	D	I	T	S	Z	X	Ac	X	P	X	Cy

O — Overflow flag
D — Direction flag
I — Interrupt flag
T — Trap flag
S — Sign flag
Z — Zero flag
Ac — Auxiliary carry flag
P — Parity flag
Cy — Carry flag
X — Not used

4. Explain the segmented memory in 8086 (8 marks)

- The address bus of 8086 is 20 bits. So it can address 2^{20} locations = 1 MByte locations (considering one location as 1 Byte)
- But the registers, ALU and Data bus is only 16 bit.
- For appropriate use of 1MB space, the whole memory is divided into segments and each segment is of size 64 KB. 16 bits of the address is enough to address any location in this segment because 2^{16} = 64 Kilo bytes.
- There can be 16 such segments in the memory.
- To identify one of these 16 segments the remaining 4 bits of address is used. (2^4 = 16), altogether which adds up to 20 bit address.
- This 20 bit address is calculated in ** a special address conversion unit in 8086. from 16 bit registers.

a) How effective address is calculated in 8086 (2 marks).

- The address in each segment ranges from 0000 to FFFF.
- The effective address is the original address that has to be used to address the memory which is 20 bit. (Also known as physical address)

- The effective address is calculated from Segment Base registers CS, DS, ES & SS & offset
- Segment Base register store the base address of each segment.
- The Segment base address is shifted fours times towards left to obtain the 20 bit base address and is then added to offset address as shown below.

Segment Base address = 1005 H.
offset address = 5555 H.

Segment address → 0001 0000 0000 0101
(shifted four times left) → 0001 0000 0000 0101 0000 +
offset → 0101 0101 0101 0101

0001 0101 0101 1010 0101
1 5 5 A 5

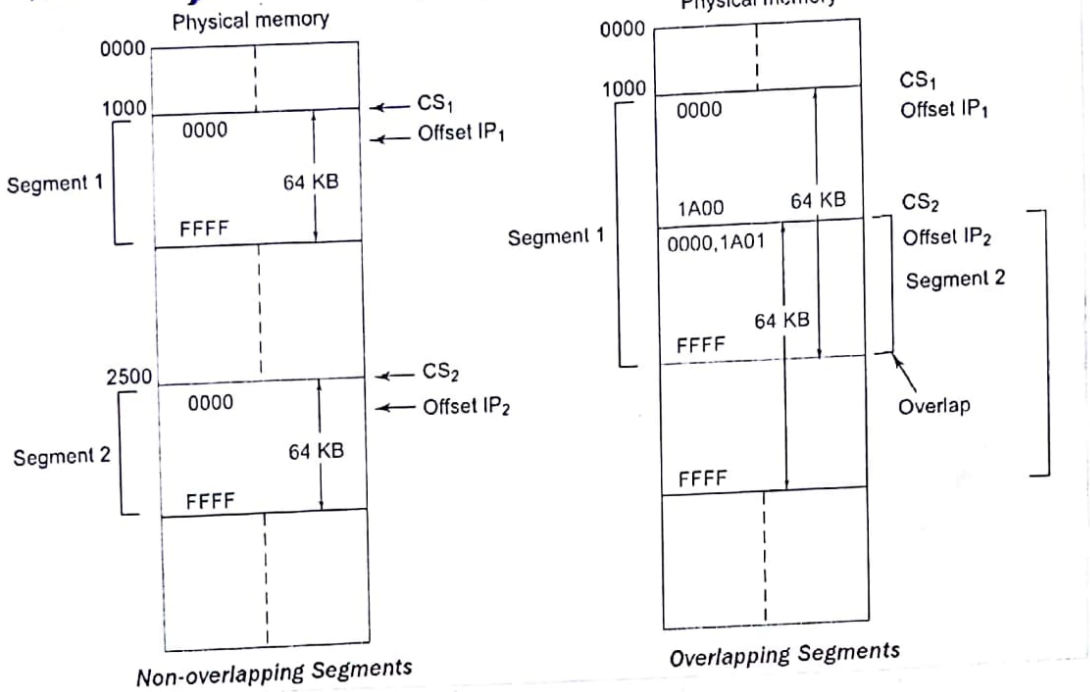
The offset address can be in IP, BX, SI, DI, SP, BP or may be in instruction as 16 bit value.

b) Describe the advantages of using Segmented memory. (2 marks)

1) Allows 1MB memory space even though the actual address to be handled is of 16 bit.

2) Data Protection :- Allows Code, Data & Stack in different parts of the memory.

3) Provision for relocation :- Allows program and data to be put into different parts of the memory each program is executed.



5. Describe the architecture of 8086. (10 marks).

- 8086 is a bit processor with 16 bit registers, that supports segmented memory with 20 bit addressing.
- The whole architecture of 8086 is divided into
  a) BIU - Bus Interface unit.
  b) EU - Execution Unit.

BIU - It contains circuit for physical address calculation and instruction byte queue. It has
a) Address Conversion Mechanism - It has a shifter and an adder to calculate Physical address of a effective address.
b) Segment Registers. - CS, DS, ES, SS
c) Instruction Pointers. - IP.

d) 6 byte Prefetch queue.

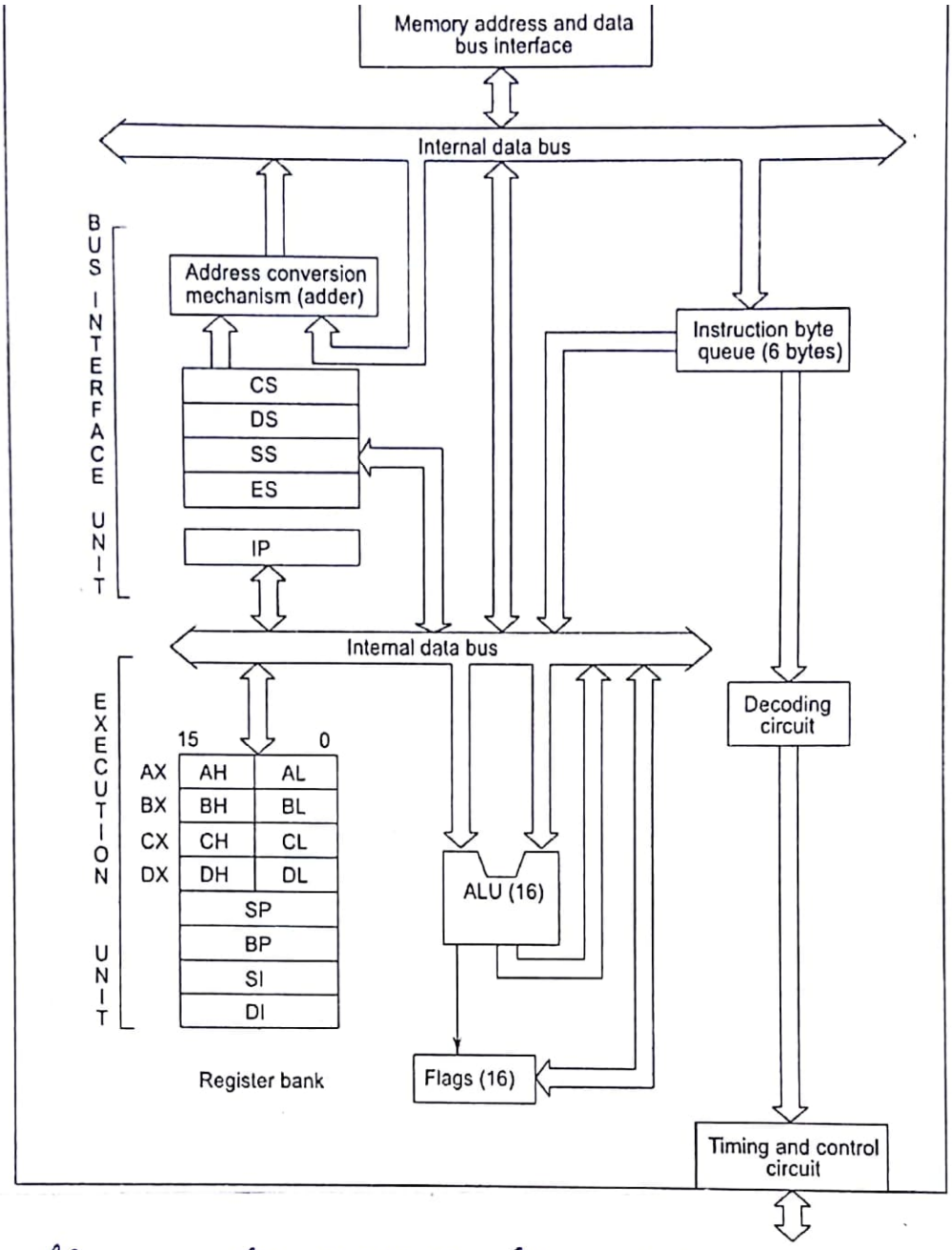
EU :- It contains all logical units required for arithmetic & logical calculation in ALU. It contains the following

a) 16 bit ALU
b) 16 bit general Purpose registers - AX, BX, CX, DX
c) 16 bit Pointer registers - SP & BP.
d) 16 bit Index Registers - SI & DI
e) Decoding Unit :- Decodes the opcode bytes issued from the instruction byte queue.
f) Flag Register.
g) Timing and Control circuit - it desires the necessary control signals to execute the instruction

Buses :- It connects different logical units in BIU and EU and also with external units. There are two types of buses.

a) Data bus :-
This carries data in between registers, ALU, queue and external devices. It is of 16 bit.

b) Address bus :-
It carries 20 bit address and is of 20 bits of size. It basically connects external memory and address Conversion unit.



6. Explain the flag register of 8086. (6 marks)

It has two functionalities.

a) Condition code or status flag
b) Machine control flag.

Condition code flags:- It reflects the results of the operation performed by ALU.

Control flag:- It controls processor operations. They are direction flag (D), Interrupt flag (I) and Trap flag (I).

Flags in Detail:-

S- Sign flag - when the result of computation is -ve

Z- Zero flag :- when result is zero or comparison matches.

P- Parity :- If the lower byte of the result contains even number of 1s.

C- Carry :- When there is a carry from MSB during addition or borrow during subtraction.

T- Trap :- Single step execution.

I- Interrupt :- Maskable interrupts can interrupt cpu only if I = 1.

D- Direction :- Used by String instruction.
when 0 > String is processed from lower address to higher address.
- Auto incrementing.
when 1 > - Auto decrementing -

O- overflow :- If the result of signed operation overflows to sign bit.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	O	D	I	T	S	Z	X	Ac	X	P	X	Cy

O — Overflow flag
D — Direction flag
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S — Sign flag
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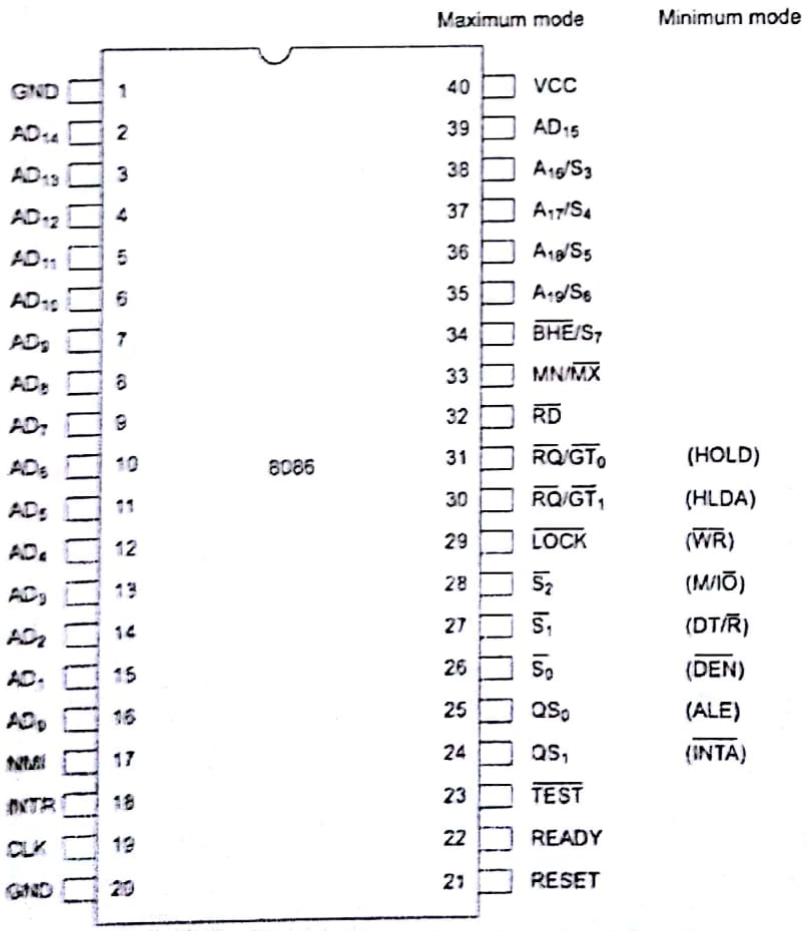
P — Parity flag
Cy — Carry flag
X — Not used

7. Explain the signals of 8086 with its pin configuration (10 marks)

8086 processor is packaged in 40 bit Ceramic Dual In line package or plastic package

The pins of 8086 are of three category.

a) Pins that pass signals having common function
b) Signals that have special function during minimum mode.
c) Signals that have special function during maximum mode.



AD_{15} - AD_0 - Time multiplexed address / data lines.
- Address available during T_1
- Data " during T_2, T_3, T_w & T_4

A_{19}/S_6, A_{18}/S_5, A_{17}/S_4, A_{16}/S_3

- There are time multiplexed address/status line.
- Address available during T_1
- Status " " T_2, T_3, T_W & T_4.

S_4	S_3	Indication
0	0	Alternate Data.
0	1	Stack
1	0	Code or None.
1	1	Data.

- S_3 & S_4 together shows which segment is used.

S_5 - denotes status of I flag.

S_6 - Always low.

$\overline{BHE}/S_7$ - Bus high enable / Status.

- Combination of BHE and A_0 denotes which memory bank is selected during T_1
- S_7 is available during T_2, T_3, T_W & T_4 which is not used.

$\overline{BHE}$	A_0	Indication.
0	0	Whole word
0	1	Upper byte from or to odd address.
1	0	Lower byte from or to even address.
1	1	None.

$\overline{RD}$ - Read.

- Reading from Memory or Peripheral device.

$\overline{WR}$ - Write.

- Writing to Memory or Peripheral device.

READY -

- acknowledgment from slow devices or memory that have completed data transfer.

INTR - Interrupt Request.

- level triggered interrupt pin.
- hardware interrupt.
- Maskable using I bit in flag.

NMI - Non Maskable Interrupt.

- Non Maskable.
- Edge triggered.
- High Priority.
- hardware Interrupt.

TEST -

- Examined by WAIT instruction.
- If TEST is low execution continues, otherwise goes into idle state.

RESET

- To restart the processor execution from FFFFOH.
- The signal should be high active atleast for 4 clock cycles.

CLK - Clock.

- Provides basic timing for processor operation.

Vcc - +5V

GND. - Ground.

MN/$\overline{MX}$ - It decides whether the processor works in minimum mode or maximum mode.

Pin functions for minimum mode operation.

M/$\overline{IO}$ – If high Memory operation
If low IO operation.

$\overline{INTA}$ – Interrupt acknowledge

ALE – Address latch enable.
- The signal that latches address bits in 74LS373 latches during T_1 and makes the $AD_0 - AD_{20}$ ready for data/status transfer.

DT/$\overline{R}$ – Data transmit / Receive.
- If high it denotes processor sends out data
- If low " receive the data.

DEN – Data Enable.
- denotes the availability of data during T_2 to T_4.

HOLD – Indicates another master is requesting processor bus.

HLDA – If the processor release its bus to external device.

Conditions to release bus.
1) Request occurs before T_2 of current cycle.
2) Current cycle is not operating over lower byte of a word.
3) Current cycle is not a Interrupt ack
4) Lock is not executed.

Pin functions for maximum mode operation.

S_2	S_1	S_0	Indication.
0	0	0	Interrupt acknowledge.
0	0	1	Read I/O Port.
0	1	0	Write I/O Port
0	1	1	Halt.
1	0	0	Code access.
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive.

LOCK :-

It indicates that other bus masters will be prevented from gaining access the processor bus.

$\overline{QS_0}, \overline{QS_1}$ - Queue Status.

- Denotes the status of the Prefetch Queue.

QS_1	QS_0	Indication.
0	0	No operation.
0	1	1st byte of the opcode from queue.
1	0	Empty queue.
1	1	Subsequent byte from queue.

$\overline{RQ}/\overline{GT_0}$, $\overline{RQ}/\overline{GT_1}$ - Request Grant.

- It request the process bus from other CPU by other bus masters.
- If the request is granted it is notified through signal GT.
- $\overline{RQ}/\overline{GT_0}$ is having high priority.

8. Explain pipelining is performed in 8086.

- Pipelining is prefetching of instruction while the processor is executing another instruction.
- These prefetched instructions are kept in a 6 byte queue in 8086.
- In BIU does this prefetching and EU does execution and both can work independently.
- In 8086 few instructions are 1 byte and 2 byte. The length of instruction will goes upto 6byte. The queue can accomodate this.
- The queue is updated (push the element to front) whenever a byte is emptied.
- The fetch of instruction happens only if two byte are empty.
- The QS_0 and QS_1 are queue status bits that denotes the operation performed.

9. Describe the Physical Memory Organisation of 8086 (5marks)

1MB Space supported by 8086 is divided into odd address bank and even address bank.

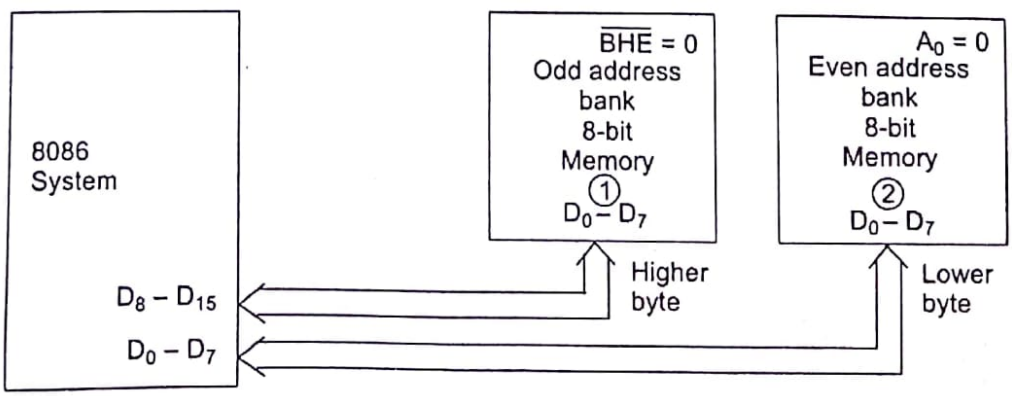


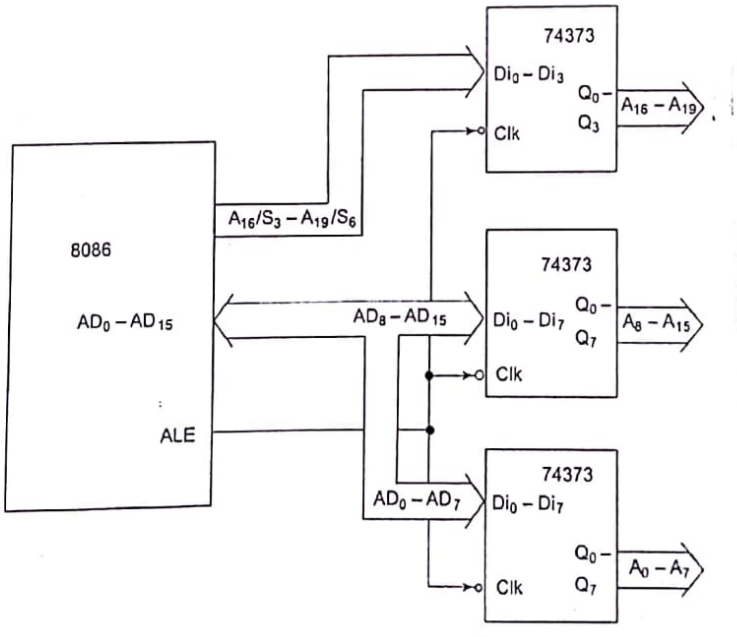
Fig. 1.7 *Physical Memory Organisation*

- Byte data through even address is transfered through $D_7 - D_0$.
- Byte data through odd address is transfered through $D_8 - D_{15}$
- The instructions can be of 1 byte, 2 byte or more than that.
- If we want access a single instruction of 2 bytes in a single cycle we have to keep that in memory starting from even address. So that first even address fetch the 1st byte of the instruction and then $D_8 - D_{15}$ fetches the second byte.
- Signals BHE & A_0 denotes which bank is currently accessed.
- It also provides provision to access single bytes either from odd address or even address.

10. How I/O addressing is done in 8086? (3 marks)
- No: of bits in address is 16 bits.
- So the no: of addresses possible or the no: of I/O registers that can be addressed is $2^{16} = 64K$
- These 16 bit address can be provided through $A_0 - A_{15}$ for T_1
- During I/O $A_{16} - A_{19}$ are in logic 0.
- During T_2, T_3, T_W and T_4 I/O address is latched by ALE.

11. Illustrate the logical circuit connection for the multiplexed system bus in 8086? (5 marks)

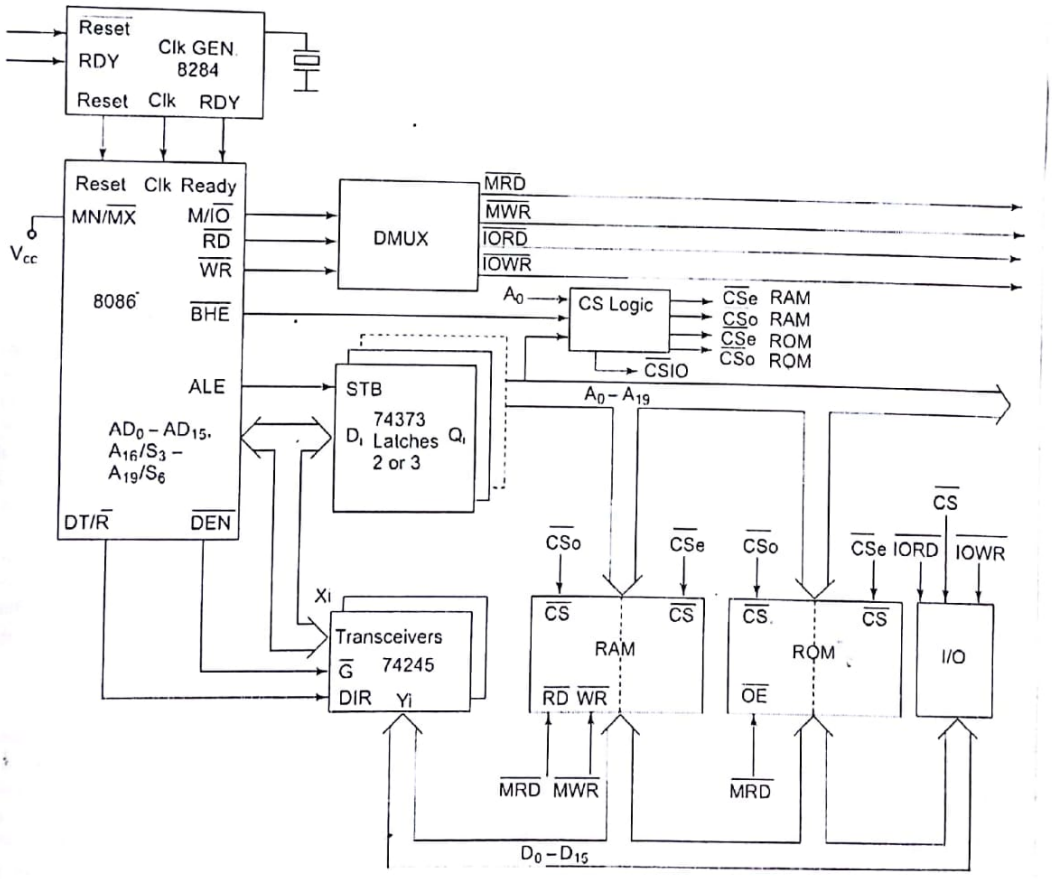
- 8086 has 20 bit multiplexed Address/Data Bus. - $AD_0 - AD_{15}$, $A_{16}/S - A_{19}/S$
- At T_1 $A_0 - A_{15}$ and $A_{16} - A_{19}$ transfer address.
- During T_2, T_3, Tw and T_4 $A_0 - A_{15}$ function as $D_0 - D_{15}$ and transfer Data.
- During T_2, T_3, Tw and T_4 $A_{16} - A_{19}$ - function as Status lines S_3, S_4, S_5, S_6
- After T_1 since the system bus change its functionality it store this address when processor issues ALE signal. The address bits are stored in latches as shown below.



Latching 20-Bit Address of 8086

12. Explain the minimum mode operation of 8086. (10 marks)

- In minimum mode operation there will be only a single processor.
- The other logical units along with this processor are latches, transbeceivers, clock generator, memory and I/O devices. Chip selection logics are also used. The complete connection in minimum mode operation is shown below.
- In minimum mode operation MN/MX pin is set to 1.

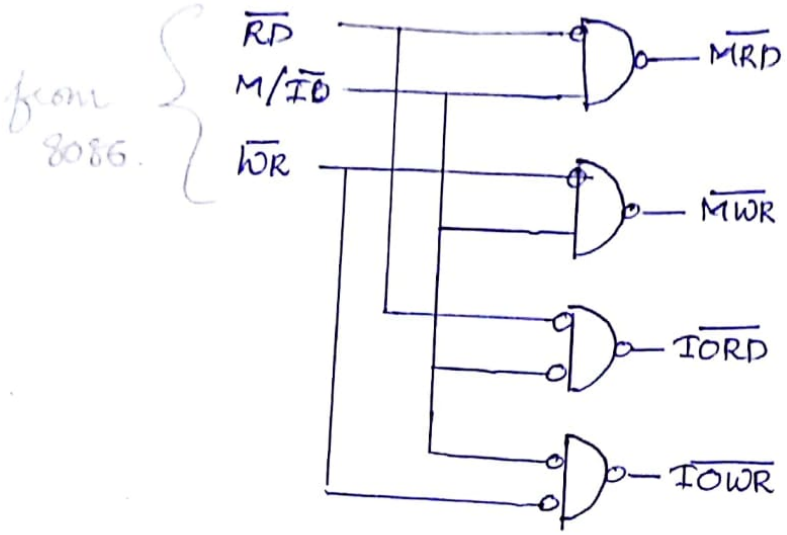


Minimum Mode 8086 System

Functionalities of additional chips :-

1. clk - That provides clock signal to 8086.
2. DMUX - That multiplexes M/$\overline{IO}$, $\overline{RD}$, $\overline{WR}$ signals to generate
   - $\overline{MRD}$ - Memory Read.
   - $\overline{IORD}$ - IO Read
   - $\overline{MWR}$ - Memory Write.
   - $\overline{IOWR}$ - IO Write.

   The internal ckt can be as follows:-



3. 74 LS 373 Latches:-
   To latch the address bits after receiving ALE signal.

4. CS Logic - Chip Select
   To select RAM and ROM
   - $\overline{CS_e}$ - To select Even memory of ROM & RAM
   - $\overline{CS_o}$ - To select odd memory of ROM or RAM.

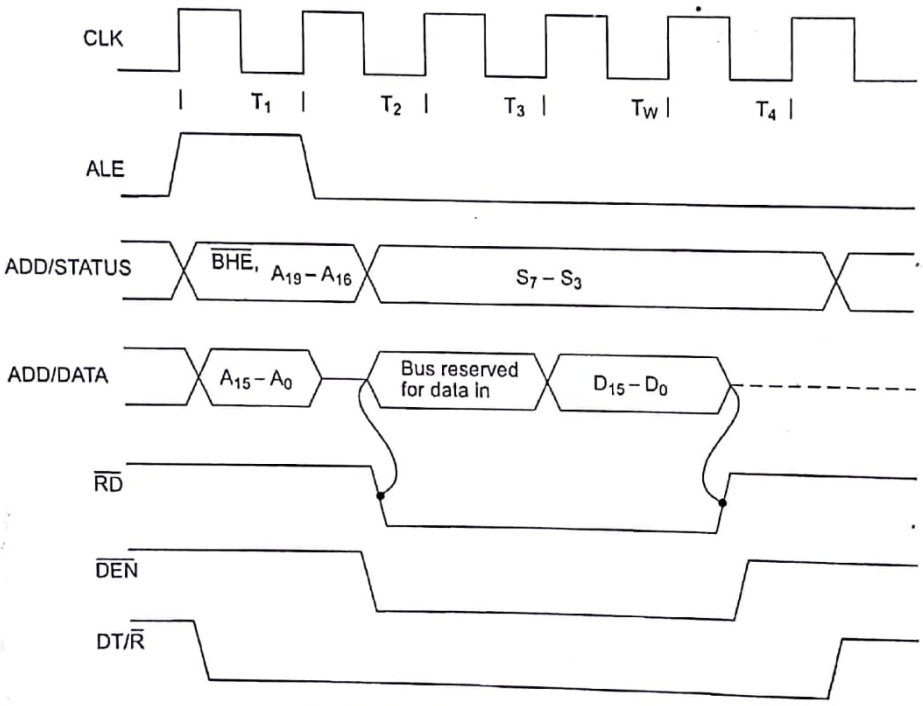
5. Transreceivers - 74245
   - Bidirectional buffers or data amplifiers.
   - It separate data from address bus.

- It works according to the signal DEN and DT/$\overline{R}$
- DEN denotes data is available
- DT/$\overline{R}$ denotes to collect data from 8086 or to give data to data bus.

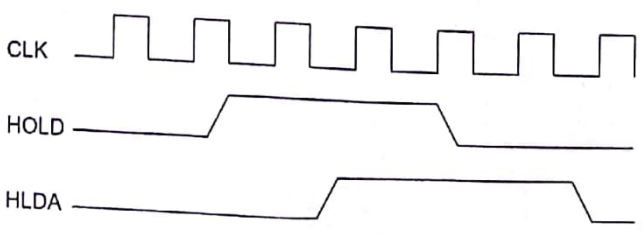
  DT means 8086 ready to transfer.
  $\overline{R}$ means " " receive.

6. RAM, ROM and I/O chips.
   - for memory and I/O.

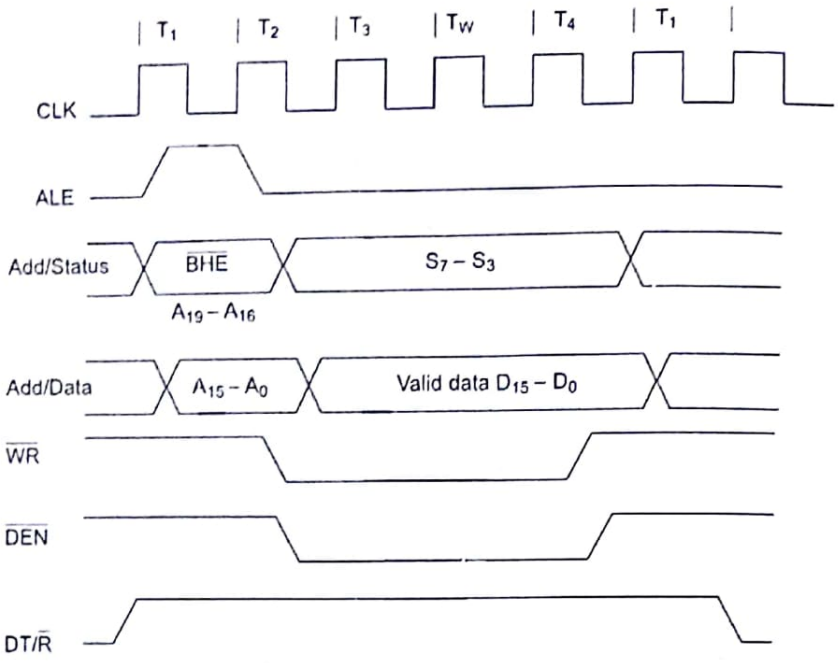
The timing diagram describes the 8086 operation in minimum mode.



Read Cycle Timing Diagram for Minimum Mode



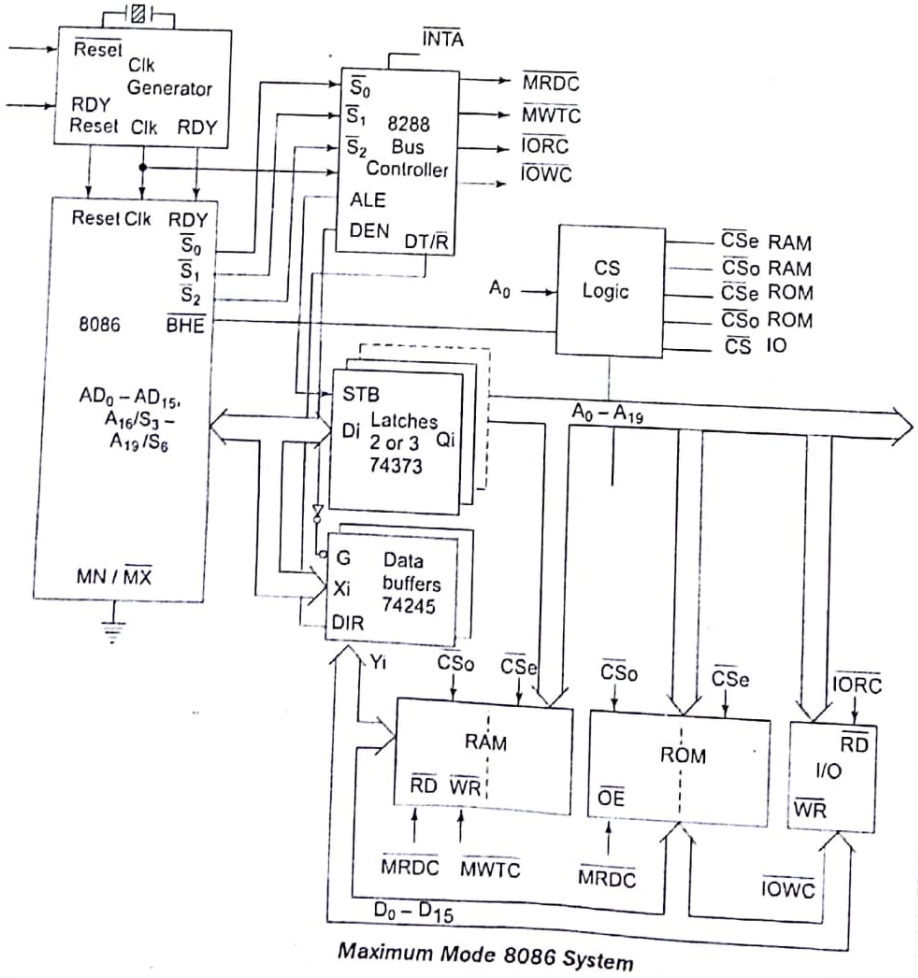
Bus Request and Bus Grant Timings in Minimum Mode System



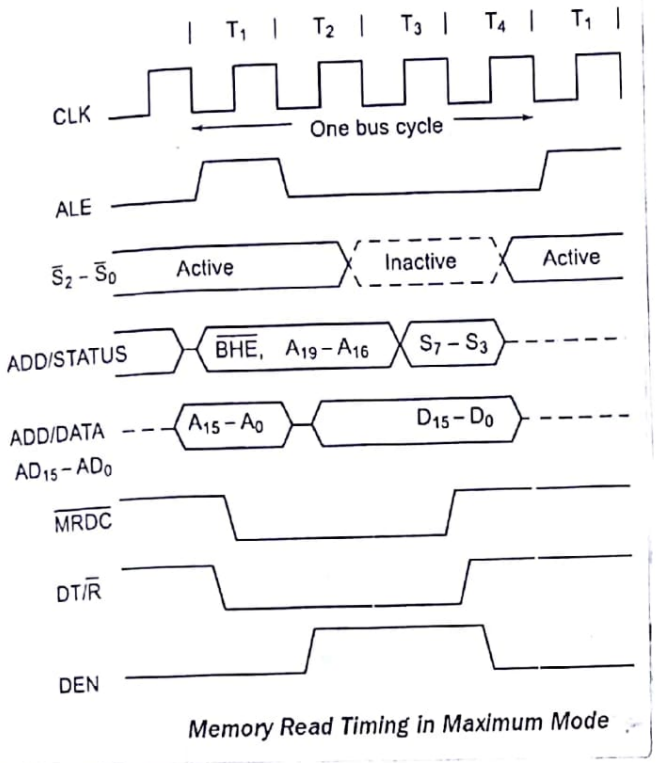
Write Cycle Timing Diagram for Minimum Mode Operation

13. Explain the maximum mode operation of 8086 (10 marks)

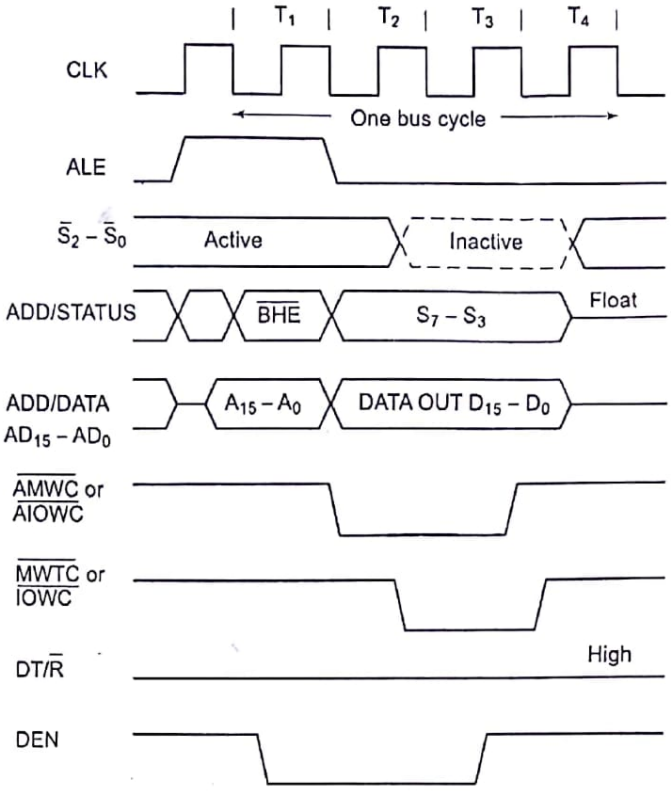
- 8086 operates in maximum mode by strapping MN/MX to gnd
- In maximum mode there will be more than one processor.



Maximum Mode 8086 System



Memory Read Timing in Maximum Mode



Memory Write Timing in Maximum Mode

- the system configuration in 8086 is shown in figure.

1) the control signals required for Memory and I/O operations are generated with 8288 Bus Controller. It uses S_0, S_1, S_2 of 8086 to generate to generate the following commands.

$\overline{MRDC}$ - Memory Read Command
$\overline{MWTC}$ - Memory Write Command
$\overline{IORC}$ - IO Read Command
$\overline{IOWC}$ - IO Write Command

Advanced Signals (activated one clock cycle earlier)

$\overline{AIOWC}$ - Advanced IO Write
$\overline{AMWTC}$ - Advanced Memory Write.

14. What is the difference between maximum mode and minimum mode operation of 8086.

MAXIMUM MODE	MINIMUM MODE
• MN/$\overline{MX}$ connected to ground	• MN/$\overline{MX}$ connected to +5V
• There are multiple processors.	• There is only a single processor.
• Control signals for Memory and I/O has to be generated through an external bus controller.	• Control signals are generated by 8086.
• More expensive	• Least expensive.
• Control signals available are QS_1, QS_0, $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ LOCK, $\overline{RQ}/GT_0$, $\overline{RQ}/GT_1$	• Minimum mode signals are $\overline{INTA}$, ALE, DT/$\overline{R}$, $\overline{DEN}$, M/$\overline{IO}$, $\overline{WR}$, HOLD, HLDA.

15. Compare 8086 and 8088.
- There was a ~~real~~ need for an 8 bit processor that works along with other 8 bit peripherals but with a programming ability provided by 8086. And thus 8088 was produ

8086	8088
• Data bus is 16 bits	• Data bus is 8 bits.
• Available clock speeds - 5 MHz, 8 MHz & 10 MHz.	• 5 MHz, 8 MHz
• Memory Capacity - 512 KB	• 1 MB
• It has M/$\overline{IO}$ pin	• while 8088 has $\overline{M}$/IO pin
• It has $\overline{BHE}$ signal	• It has Status Signal (SSO)
• It can read 8 bit or 16 bit	• It can read only 8 bit
• 6 byte queue	• 4 byte queue.
• Memory is divided into banks	• No banks in memory.
• Maximum supply current is 360 mA	• 340 mA.